BAKER COLLEGE
STUDENT LEARNING OUTCOMES

CIS 4010 Advanced Computer Architecture
3 Semester Hours

Student Learning Outcomes & Enabling Objectives

1. Evaluate the performance of a given microprocessor architecture using several measures.
    a. Understand the how the number of results per cycle relates to clock cycles
    b. Understand maximum program or data size
    c. Apply cost analysis relevant to number of cycles based on maximum data size.

2. Examine the philosophy of various benchmark programs related to microprocessor performance and evaluate the impact of that philosophy on the results of the tested architecture.
    a. Identify specific applications for benchmark concepts attributable to SPEC95.
    b. Identify specific applications for benchmark concepts attributable to MIPS.
    c. Identify specific applications for benchmark concepts attributable to Amdahl's Law.

3. Examine the evolution of instruction sets in HLL, RISC and CISC architectures.
    a. Identify specific application for instructions in HLL, RISC and CISC architecture.
    b. Understand advantages and disadvantages for RISC and CISC.

4. Examine proficiency and understanding of principles of binary arithmetic operations.
    a. Identify the application of modern ALU designs as they relate to Logical manipulation, shifting, bit-by-bit operations of AND, OR, NOT.
    b. Apply Multiplication and division algorithms, shift/add and shift/add/subtract
    c. Identify and apply floating-point numbers and normalization on construction of ALU.

5. Explain the performance improvement incurred in an architectural system through the use of parallel, pipelined, and multiprocessor designs.
    a. Identify all architectural design systems such as parallel, pipeline and multiprocessor.
    b. Apply all architectural design systems such as parallel, pipeline and multiprocessor.

6. Assess the philosophy of various benchmark programs related to microprocessor performance.
    a. Comparing and contrasting different designs.
    b. Understanding the impact of branch prediction design on choices made by a programmer.

7. Evaluate the effectiveness of hierarchical memory designs.
    a. Analyzing relationships of memory levels including cache and virtual memory.
    b. Analyzing memory levels in terms of speeds, sizes, and costs.
    c. Analyzing the performance penalties incurred in memory misses.
    d. Comparing and contrasting write-through cache with write-back cache in modern designs.

8. Evaluate and describe assembler and linker functions.
    a. Understand when and how to use assemblers and the disadvantages.
    b. Understand how linkers allow separate compilation of different pieces of a program.
    c. Understand how a program loads into memory and memory usage.
    d. Understand procedure call conventions.
    e. Understand exceptions and interrupts are handled by registers and memory.

These SLOs are approved for experiential credit.

Effective: Fall 2017